Details of Evening Certificate course offered by Department of Electronics and Communication Engineering:

Name of the Course: CAD of VLSI Chip Design

Duration of the Course: 1Year

Short Description of the course: The demand for digital VLSI design services is intricately linked to the overall expansion of the semiconductor industry. With projections indicating that the global semiconductor industry could reach a trillion-dollar valuation by 2030, there is a growing imperative to create efficient and specialized Digital Integrated Circuits. This certification course in CAD of VLSI Chip Design aims to enhance participants' proficiency in crafting digital integrated circuits, encompassing areas such as RTL (Register Transfer Level) design, synthesis, verification, and testing. Additionally, it provides hands-on exposure to industry-standard tools and design methodologies employed in digital VLSI design, including CAD tools, hardware description languages (HDLs), and simulation tools. Well qualified and experienced faculty members of the Electronics & Communication Engineering department at Sister Nivedita University, will equip participants with the requisite skills and knowledge to pursue career opportunities in digital VLSI design across semiconductor companies, electronics design firms, or research institutions.

Total Credit: 85

Proposed Course Fee: Rs. 50,000.00

Eligibility : B.Sc. with mathematics as one of Pass paper/Diploma in Electronics, Electrical, Instrumentation, Computer Science/ B.Tech. in Electronics, Electrical, Instrumentation, Computer Science.

Mode : Hybrid

Proposed Curriculum:

Sr. No.	Module Title	Duration (Hours)
1	**Review of Digital Electronics** • Combinational Circuit Design • Sequential Circuit Design • Design of controller and Data path units • State Machines • Controller Design using FSMs & ASMs • Design Examples & Case Studies	15

2	**Introduction To VLSI** • Need, Scope, Use and History of VLSI • Introduction to Chip Design Process • Description of Hardware Description Languages • Applications of VLSI • VLSI Design Flow • Moore's Laws • VLSI Design Flow and Y-Chart • Front-Back End VLSI Design	10
3	**Verilog HDL** • Introduction to Verilog HDL & Hierarchical Modeling Concepts • Lexical Conventions & Data Types • System Tasks & Compiler Directives • Modules, Ports and Module Instantiation Methods • Modeling methods.	20
4	**FPGA Architecture and Prototyping** •Introduction to Programmable Logic and FPGAs •Popular CPLD & FPGA Families •Architecture of popular Xilinx and Altera FPGAs •FPGA Design Flow •Implementation Details •Advanced FPGA Design tips •Logic Synthesis for FPGA • Design problems(Mini Project)	20

5.	**Introduction to design tools** • Schematic Capture using Virtuoso Schematic Editor • Symbol Creation • Testbench Creation using Virtuoso Schematic Editor • Functional Simulation • Layout Design using Layout Editor • Physical Verification which includes DRC & LVS • Parasitic Extraction • Post Layout Simulation	20

Approximate expenditure: This course will require some hardware and software tools for VSLI Design which will cost approximately **Rs. 13,00.000.00** for 10 users' licence. However, these hardware and software will also be required by our B.Tech and M.Tech. students of ECE and CSE.

Some Experts from Industry/academic Institutes will also deliver lectures which may cost approximately **Rs. 2,00.000.00**

Total expenditure: Rs. 15,00,000 approximately